

U.S. Department of Commerce, Patent and Trademark Office		Atty. Docket No.	Application No.
		NS-5127-1D US	10/699,221
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Applicant(s)	Confirmation No.
Substitute Form PTO 1449		Bulucea, Constantin	2799
MAY 09 2005		Filing Date	Group
		31 October 2003	2814

## U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
DF	AA	2002/0074589	06/2002	Benaissa et al.	257	312	
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	AD						
	AE						
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	AH						
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	AE						
	AF						
	AG						
	AH						

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		Document	Date	Country	Class	Subclass	Translation
	AI						
	AJ						
	AK						
	AL						
	AM						

## OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

DF	AN	Takeuchi et al, "A New Multiple Transistor Design Methodology for High Speed Low Power SOCs," <u>IEDM Technical Digest</u> , December 2001, pages 22.6.1 - 22.6.7
	AO	
	AP	

Examiner Benaissa Date Considered 12/18/05

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

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## U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
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	AC	5,504,376	04/1996	Sugahara et al.	257	768	
	AD	5,659,185	10/1997	Iwamuro	257	138	
	AE	5,977,591	11/1999	Fratin et al.	257	344	
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## Foreign Patent Documents

		Document	Date	Country	Class	Subclass	Translation	Yes	No
DC	AI	4-199682	07/1992	Japan	257	365			X
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## OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

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Examiner *Dee Shan*Date Considered *12/1/2005*

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U.S. Department of Commerce, Patent and Trademark Office		Atty Docket No.	Application No.
		NS-5127-1D US	Unknown
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)		Applicant	Confirmation No.
		Constantin Bulucea	Unknown
		Filing Date	Group
		Herewith	Unknown

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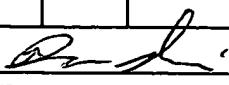
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
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DF	AH	Andreani, et al., "A 1.8-GHZ CMOS VCO Tuned by an Accumulation-Mode MOS Varactor," <u>IEEE Intl. Symposium on Circuits and Systems</u> , 28 – 31 May 2000, pp. I-315 – I - 318.
DF	AI	Grove, <u>Physics and Technology of Semiconductor Devices</u> (John Wiley & Sons), 1967, pp. 263 – 305.
DF	AJ	Grove, et al., "Effect of Surface Fields on the Breakdown Voltage of Planar Silicon <i>p-n</i> Junction," <u>IEEE Trans. Electron Devices</u> , vol. ED-14 ,1967, pp. 157 – 162.
DF	AK	Grove, et al., "Surface Effects on <i>p-n</i> Junctions: Characteristics of Surface Space-Charge Regions Under Non-Equilibrium Conditions," <u>Solid-State Electronics</u> , Vol. 9, 1966, pp. 783 - 806.
DF	AL	Kral, et al., "RF-CMOS Oscillators with Switched Tuning," <u>Procs. IEEE Custom Integrated Circuits Conference</u> , 1998, pp. 555 – 558.
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DF	AO	Moll, "Variable Capacitance With Large Capacity Change," <u>IRE Wescon Conf. Rec.</u> , Vol. 3, 1959, pp. 32 - 36.

Examiner 

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)		Applicant	Confirmation No.
		Constantin Bulucea	9448
		Filing Date	Group
		January 18, 2002	2814

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## OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

DF	AH	Ng, <u>Complete Guide to Semiconductor Devices</u> (McGraw Hill), 1995, pp. 11 - 22.
PF	AI	Razavi, <u>Design of Analog CMOS Integrated Circuits</u> (McGraw Hill), 2001, pp. 495 - 525.
DF	AJ	Rusu et al., "Deep-Depletion Breakdown Voltage of Silicon-Dioxide/Silicon MOS Capacitors," <u>IEEE Trans. Elec. Devs.</u> , March 1979, pp. 201 - 205.
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DF	AM	Svelto, et al., "A Three Terminal Varactor for RF IC's in Standard CMOS Technology," <u>IEEE Transactions on Electron Devices</u> , Vol. 47, 2000, pp. 893 - 895.
DF	AN	Warner, Jr., et al., <u>Transistors - Fundamentals for the Integrated-Circuit Engineer</u> (John Wiley & Sons), 1983, pp. 320 - 321.
DF	AO	Wong et al., "A Wide Tuning Range Gated Varactor," <u>IEEE J. Solid State Circs</u> , May 2000, pp. 773 - 779.
Examiner	<i>John</i>	Date Considered 12/19/05

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